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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,608	12/23/2004	Salvatore Pappalardo	02-CT-104/DP	9027

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EXAMINER	
CARTER III, ROBERT E	
ART UNIT	PAPER NUMBER
2609	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/518,608	PAPPALARDO ET AL.	
	Examiner	Art Unit	
	Robert E. Carter	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/23/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

1. Claims 1-10 are rejected under 35 U.S.C. 102(a) as being anticipated by applicant's admitted prior art (Fig. 1).

As for claim 1,

The admitted prior art (Fig. 1) teaches:

A system for driving rows of a liquid crystal display comprising: at least one module (Fig. 1) for driving one single row of said liquid crystal display, said module comprising an inverter (T10, T7) operating in a supply path between a first and a second supply line of said system, said first supply line comprising first means (T10, T9) capable of coupling it to a first (VLCD) or to a second (VA) supply voltage and said second supply line comprising second means (T8, T7) capable of coupling it to a third (VB) or to a fourth (VSS) supply voltage, said inverter (T10, T7) being driven by a logic circuitry (1, C1) and

providing a drive signal for one single row of said liquid crystal display.

As for claim 2,

The admitted prior art (Fig. 1) teaches all the limitations of claim 1, and further teaches: Wherein said inverter comprises a PMOS transistor (T10) and a NMOS transistor (T7).

As for claim 3,

The admitted prior art (Fig. 1) teaches all the limitations of claim 1, and further teaches: Wherein the value of said first supply voltage (VLCD) exceeds said second supply voltage (VA), the value of said second supply voltage (VA) exceeds said third supply voltage (VB), and the value of said third supply voltage (VB) exceeds said fourth supply voltage (VSS) (Paragraph [0017], lines 1-3).

As for claim 4,

The admitted prior art (Fig. 1) teaches all the limitations of claim 1, and further teaches: Wherein said first (T10, T9) and second (T8, T7) means are controlled by a logic signal (LOW_FRAME) that controls respectively the connection of the first supply line to said first (VLCD) or to said second (VA) supply voltage and the connection of the second supply line to said third (VB) or to said fourth (VSS) supply voltage according to whether a frame is uneven or even.

As for claim 5,

The admitted prior art (Fig. 1) teaches all the limitations of claim 4, and further teaches: Wherein said logic circuitry (1, C1) comprises a logic device (1) capable of supplying an additional input logic signal (A) to an elevator device (C1) capable of raising the level of said additional logic signal for driving said inverter (T10, T7).

As for claim 6,

The admitted prior art (Fig. 1) teaches:

A module for driving a row in a liquid crystal display (Fig. 1) comprising:

an inverter having first and second power terminals (T10, T7);

a first switch (T10, T9) for coupling the first power terminal of the inverter to a first (VLCD) or a second (VA) supply voltage; and

a second switch (T8, T7) for coupling the second power terminal of the inverter to a third (VB) or fourth (VSS) supply voltage, wherein the inverter is driven by a logic circuit (1, C1) and provides a drive signal for the row.

As for claim 7,

The admitted prior art (Fig. 1) teaches all the limitations of claim 6, and further teaches: Wherein the inverter comprises a PMOS transistor (T10) and a NMOS transistor (T7).

As for claim 8,

The admitted prior art (Fig. 1) teaches all the limitations of claim 6, and further teaches:

Wherein the first and second supply voltages have different values, and the third and fourth supply voltages have different values (Paragraph [0017], lines 1-3).

As for claim 9,

The admitted prior art (Fig. 1) teaches all the limitations of claim 6, and further teaches: Wherein the first and second switches are driven by a logic signal (A), the state of the logic signal being determined by whether a frame is uneven or even (LOW_FRAME).

As for claim 10,

The admitted prior art (Fig. 1) teaches all the limitations of claim 9, and further teaches: Further comprising a level shifter (C1).

Conclusion

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Shigeta (US Patent # 6,091,385) discloses a driving circuit with multiple driving voltages.

Yanagi et al. (US Patent # 5,929,847) discloses a driving circuit with a logic circuit, a level shifter, and an inverter.

Imamura (US Patent # 5,903,260) discloses a driving circuit with multiple driving voltages.

Ebihara (US Patent # 5,841,412) discloses a driving circuit with multiple driving voltages.

Yumoto et al. (US Patent # 6,542,142) discloses a driving circuit with multiple driving voltages.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Carter whose telephone number is 571-270-3006. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on 571-272-7331. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

REC

Kent Chang

KENT CHANG
PRIMARY EXAMINER